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Design of High Speed Based On Parallel Prefix Adders Using In FPGA

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Abstract

The binary adder is the critical element in most digital circuit designs including digital signal processors (DSP) and microprocessor data path units. As such, extensive research continues to be focused on improving the power-delay performance of the adder. In VLSI implementations, parallel-prefix adders(also known as carry-tree adders) are known to have the best performance. However,this performance advantage does not translate directly into FPGA implementations due to constraints on logic block configurations and routing overhead. This paper investigates three types of carry-tree adders (the Kogge-Stone, sparse Kogge-Stone, and spanning tree adder) and compares them to the simple Ripple Carry Adder (RCA). These designs of varied bit-widths were implemented on a Xilinx Virtex 5 FPGA and delay values were taken from static timing analysis of synthesis results obtained from Xilinx ISE design suite 10.1. Due to the presence of a fast carry-chain, the RCA designs exhibit better delay performance up to 64 bits. The carry- tree adders have a speed advantage over the RCA as bit widths approach 256.

Keywords: Adders, KS adder, RCA,SKS adder,Simulation.

Introduction

In processors (DSP) and microprocessor data path units, adder is an important element. As such, extensive research continues to be focused on improving the power-delay performance of the adder. In VLSI implementations, parallel adders are known to have the best performance. Reconfigurable logic like Field Programmable Gate Arrays (FPGAs) has been gaining more popularity in recent years because it offers improved performance in terms of speed and power over DSP-based and microprocessor-based solutions, for many practical designs involving mobile DSP and telecommunications applications and a significant reduction in development time and cost over Application Specific Integrated Circuit (ASIC) designs. The power advantage is important with the growing popularity of mobile and portable electronics, which make extensive use of DSP functions. However, because of the structure of the configurable logic and routing resources in FPGAs, parallel-prefix adders will have a different performance than VLSI implementations [1]. In particular, most modern FPGAs employ a fast-carry chain which optimizes the carry path for the simple Ripple Carry Adder (RCA). this work was supported in part by NSF LSAMP and UT-System STARS awards. The FPGA ISE synthesis software was supplied by the Xilinx University program described. An efficient testing strategy for evaluating the performance of these adders is discussed. Several tree- based adder structures are implemented and characterized on a FPGA and compared with the Ripple Carry Adder (RCA) and the Carry Skip Adder (CSA). Finally, some conclusions and suggestions for improving FPGA designs to enable better tree-based adder performance are given. Parallel-prefix structures are found to be common in high performance adders because of the delay is logarithmically proportional to the adder width. Such structures can usually be divided into three stages:1. pre-computation,2. prefix tree 3. Post-computation.

1. Pre processing **:** This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

pi = Ai XOR Bi gi = Ai AND Bi

2. ***Carry look ahead network :***This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equations below:

Pi:j = Pi:k+1 AND Pk:j

Gi:j = Gi:k+1 OR (Pi:k+1 AND Gk:j)

3. ***Post processing*** *:*This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic given below:

Si = pi XOR Ci-1

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Parallel Prefix Adders

This section describes the basic adders used in this thesis. The adders implemented on FPGAs are the Kogge-Stone adder, ripple carry adder and sparse Kogge-Stone adder. The ripple carry adder is one of the simplest adder designs. The Kogge-Stone adder is an example of a parallel prefix adder. The internal blocks used in the adder designs are described in detail in this section.

a).*Ripple Carry Adder:*

The ripple carry adder is one of the simplest adders. It consists of a cascaded series of full adders. For example 4-bit adder can be constructed by cascading four full adders together as shown in Figure. The ripple carry adder is relatively slow as each full adder must wait for the carry bit to be calculated from the previous full adder. The worst case delay of a ripple carry adder occurs when cin propagates from the first stage to the most significant bit position. The delay for an N-bit adder is given by,

$$t_{adder} = (N-1)t_{carry} + t_{sum}$$

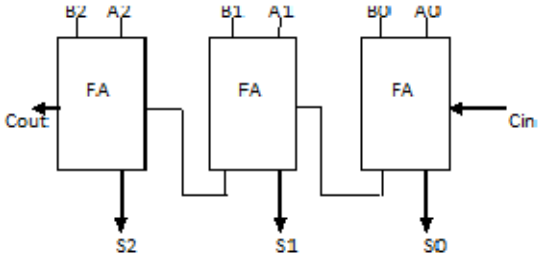

Figure 2.0: Ripple Carry Adder

b) *Kogge–Stone adder* :

The Kogge–Stone adder is a parallel prefix form carry look-ahead adder. It generates the carry signals in O(log n) time, and is widely considered the fastest adder design possible. It is the common design for high-performance adders .It takes more area to implement than the Brent–Kung adder, but has a lower fan-out at each stage, which increases performance. Wiring congestion is often a problem for Kogge–Stone adders as well.

The Kogge-Stone adder is classified as a parallel prefix adder since the generate and the propagate signals are pre-computed. In a tree-based adder, carries are generated in tree and fast computation is obtained at the expense of increased area and power. The main advantage of this design is that the carry tree reduces the logic depth of the adder by essentially generating the carries in parallel. The parallel prefix adder more favorable in terms of speed due to the O(log2*n*) delay through the carry path compared to O(*n*) for the RCA.

The Kogge-Stone adder is widely used in high-performance 32-bit, 64-bit, and 128-bit adders as it reduces the critical path to a great extent compared to the ripple carry adder. The operation of the tree-based adder can be understood using the concept of the fundamental carry operation (*fco*). This operator works on the generate and propagate pairs as defined by,

$$(g_L, p_L) \; o \; (g_R, p_R) = (g_L + p_L \cdot g_R, p_L \cdot p_R)$$

Where gL, pL are the left input generate and propagate pairs and gR, pR are the right input generate and propagate pairs to the cell. For example, in a 4-bit carry look ahead adder, the carry combination equation can be expressed as,

$$c_4 = (g_4, p_4) \; o \; [\,(g_3, p_3) \; o \; [(g_2, p_2) \; o \; (g_1, p_1)]\,]$$

$$= (g_4, p_4) \; o \; [\,(g_3, p_3) \; o \; [(g_2 + p_2 \cdot g_1, p_2 \cdot p_1)]\,]$$

$$\vdots$$

$$\vdots$$

$$= g_4 + p_4 \cdot g_3 + p_4 \cdot p_3 \cdot g_2 + p_4 \cdot p_3 \cdot p_2 \cdot g_1$$

Since the *fco* obeys the associativity property, the expression can be reordered to yield parallel computations in tree based structure,

$$c_4 = [(g_4, p_4) \; o \; (g_3, p_3)] \; o \; [(g_2, p_2) \; o \; (g_1, p_1)]$$

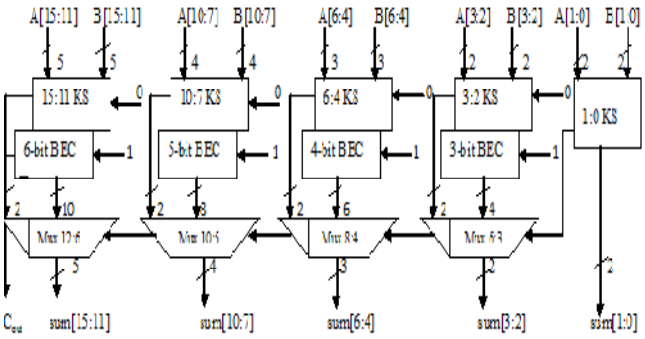

Fig:2.1 16-bit kogge-stone adder

b).sparse kogge-stone adder generator

This generates Verilog code for adders with large numbers of bits. While a complete adder would produce the output of all bits, this just outputs a series of carry bits at fixed intervals. These can be used as the carry-in bits for a series of smaller adders. This is useful in particular for FPGAs, where small ripple-carry adders can be much faster than general-purpose logic thanks to fast connections between neighbouring slices. This allows a large adder to be composed of many smaller adders by generating the intermediate carries quickly. The sparse Kogge-Stone adder consists of several smaller ripple carry adders (RCAs) on its lower half and a carry tree on its upper half. Thus, the sparse Kogge-

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Stone adder terminates with RCAs.The number of carries generates is less in a sparse Kogge-Stone adder compared to the regular Kogge-Stone adder. The functionalities of the GP block, gray cell and black cell remains exactly the same as the regular Kogge-Stone adder. The schematic for a 16-bit sparse Kogge-Stone adder is shown in Figure 2.2. Sparse and regular Kogge-Stone adders have essentially the same delay when implemented on an FPGA although the former utilizes much less resources.

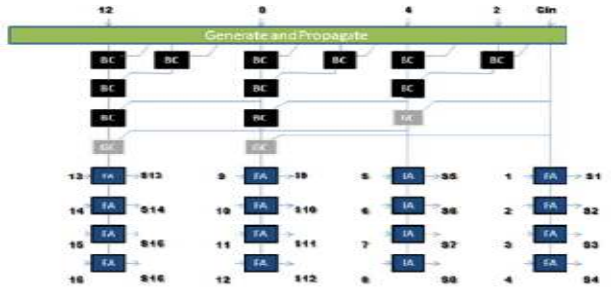

Figure 2.2: 16-bit sparse kogge-stone adder

ALLIED Work

The Basys board is a circuit design and implementation platform that anyone can use to gain experience building real digital circuits. Built around Xilinx Spartan-3E Field Programmable Gate Array and Cypress EZUSB controller, then the Basys board provides complete, ready-to-use a hardware suitable for hosting circuits ranging from basic logic devices to complex controller. A large collection of onboard I/O devices and all required FPGA support circuits are included,so the countless designs can be created without the need for any other components.Four standard expansion connectors allow designs to grow beyond the Basys board using breadboards, user-designed circuit boards, or Pmods (Pmods are inexpensive analog and digital I/O modules that offer A/D & D/A conversions, motor drivers, sensor inputs and many other features)..The Basys board work seamlessly with all versions of the Xilinx ISE tools, including the free Web Pack. It ships with a USB cable that provides power and a programming interfaces. So no other power supplies or programming cables are required.

Result

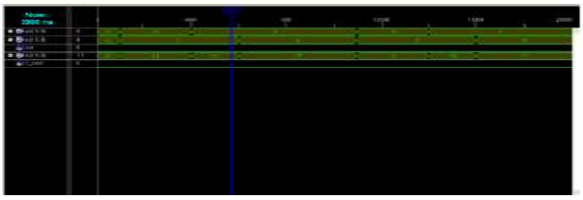

Fig:4.0 Simulation Result of 16bit RC

Fig:4.1 Simulation Results of KSA -16 bit

Experimental Result

Adder Type	Delay	No. of slices	Memory
4-bit RC	8.69 ns	4	152556 KB
4-bit KSA	9.838 ns	4	151532 KB
16-bit RC	24.686 ns	18	152556 KB
16-bit KSA	21.700 ns	21	154604 KB
16-bit SKSA	20.042 ns	22	153580 KB
128 BIT RC	162.44 ns	147	159724 KB
128 BIT KSA	26.877 ns	646	173612 KB
128 BIT SKSA	75.400 ns	272	164844 KB

Conclusion

The Above Experimental Results proved that parallel prefix adders are very high speed than normal Ripple carry Adders when it will increase the width of the adders. All adders will successfully synthesized using Xilinx9.1 synthesis tool and simulation will done using ISE simulator. We are generating a synthesis reports for Spartan 3E FPGA The replacement of prefix adders in place of Ripple Carry Adders offers great advantage in the reduction of delay.

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